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12GHz-BAND LOW-NOISE GaAs MONOLITHIC AMPLIFIERS

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ABSTRACT

One- and two-stage 12GHz-band low-noise GaAs monolithic amplifiers have been developed for use in direct broadcasting satellite receivers. The one-stage amplifier provides a less than 2.5dB noise figure with more than 9.5dB associated gain in the 11.7 to 12.7GHz band. In the same frequency band, the two-stage amplifier has a less than 2.8dB noise figure with more than 16dB associated gain. A 0.5 um gate closely-spaced electrode FET with an ion implanted active layer is employed in the amplifier in order to achieve a low noise figure without reducing reproducibility. Chip size is 1 mm x 0.9 mm for the one-stage amplifier and 1.5 mm x 0.9 mm for the two-stage amplifier.

INTRODUCTION

Recent advances in GaAs technology have made monolithic microwave integrated circuits (MMICs) more practical. Promising applications for this technology include inexpensive receiver frontends for direct broadcasting satellite (DBS) systems.[1][2] This paper describes design considerations, fabrication process and performances for newly developed one- and two-stage 12GHz-band low-noise GaAs monolithic amplifiers for use in DBS receivers. For MMICs used in DBS receivers, reproducibility improvement and chip size reduction are essential in order to achieve low cost. A low noise figure is also required for the amplifiers, because it determines the overall receiver noise figure. In this work, most efforts were focused on achieving these requirements.

FET DESIGN

The main reason for reducing reproducibility is a variation in FET characteristics caused by nonuniformity in active layers. To improve uniformity, an ion implantation technique was employed to form the active layers, although epitaxially grown active layers are believed to be better for low-noise FETs. In conventional MMICs, a recessed gate structure has been widely used for reducing unfavorable source resistance. Gate recessing process, however, degrades good uniformity for ion implanted active layers. To overcome this difficulty, a closely-spaced electrode (CSE) FET structure[3][4] was introduced. In the CSE FET, source-gate and drain-gate spacings are shortened to 0.5 um, so that source resistance can be reduced without recessing the gate. Fig. 1 is a cross-sectional SEM photograph of the FET. The gate was formed 0.5 um long by side-etching from a 1.5 um long photo-resist mask. The mask was also utilized to form ohmic electrodes. Therefore, the gate and the ohmic electrodes were self-aligned.

Although a bar shaped gate pattern is usually used in discrete low-noise FETs[5], an interdigital electrode pattern has been employed, because this pattern uses less space. The FET has four gate fingers. Total gate width is 280 um. FET threshold voltage Vt has been chosen as -1.7V. Fig. 2 shows static characteristics for the FET. Observed transconductance gm at 10mA drain current is 105mS/mm. Source resistance Rs and gate capacitance Csg are 4Ω and 0.23pF, respectively. Microwave characteristics were measured at 12GHz. Minimum noise

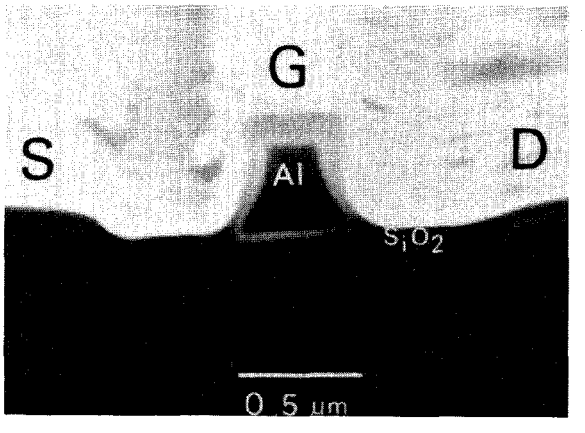

Fig. 1 CSE FET cross-sectional SEM photograph

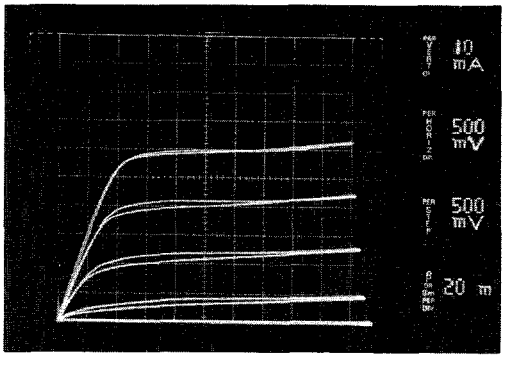

Fig. 2 CSE FET static characteristics

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figure Fmin and associated gain Ga at 10mA drain current are 1.7dB and 8.8dB, respectively. Maximum available gain (MAG) at 30mA drain current is 11.5dB. These characteristics are almost the same as for the deeply recessed epi FET[5].

In fig. 3, histograms showing Vt distributions for the CSE FET and the deeply recessed epi FET are comparatively presented. Averaged threshold voltage Vt and standard deviation σn for the CSE FET are -1.73V and 0.14V, respectively. Sample variation coefficient σn/Vt, which is a uniformity measure, is improved to about one-fourth, as compared with the epi FET.

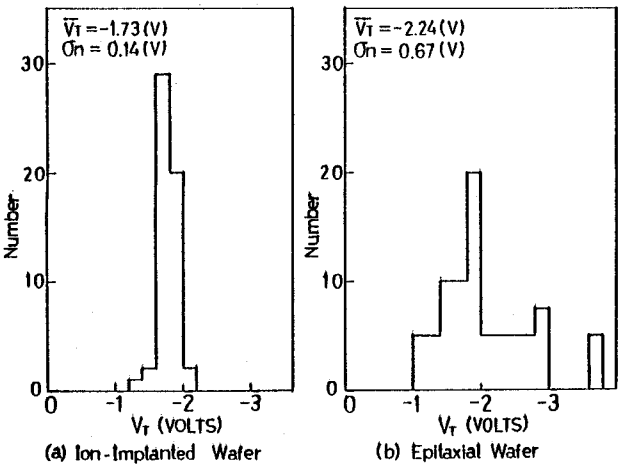

Fig. 3 Histograms showing threshold voltage distributions for CSE FET and deeply recessed epi FET

AMPLIFIER DESIGN

Fig. 4 shows a chip photograph for the one-stage amplifier. Fig. 5 shows its equivalent circuit. Chip size is 1 mm x 0.9 mm and wafer thickness is 150 um. One-section parallel and series microstrip lines are used for matching circuits. These line can also be utilized as DC bias feed lines. This arrangement allows a great savings in chip area. To retain a high Q value, a 2.5 um metallization thickness was chosen. The measured Q value for a 50 um wide line, which was mostly used in the amplifier, is 30 ~ 40 at 12GHz. As shown, the microstrip lines were folded in order to reduce the chip size. To avoid parasitic couplings, the spacings between adjacent lines were designed as large as possible.

Capacitors are MIM type, where dielectric material is SiO_2, whose relative dielectric coefficient ε_r is 4.8. Measured Q value, which is insensitive to frequency and capacitance, is around 20. All capacitors are used as DC-block or RF-short capacitors. Therefore, capacitance has been chosen larger than 2pF and thichness control for SiO_2 film is not critical.

By using measured S parameters for a discrete FET,element values in a FET equivalent circuit were derived. Based on these values, the amplifier circuit parameters were optimized by a CAD program. In the desired frequency band, which is from 11.7 to 12.7GHz, more than 9dB gain was predicted.

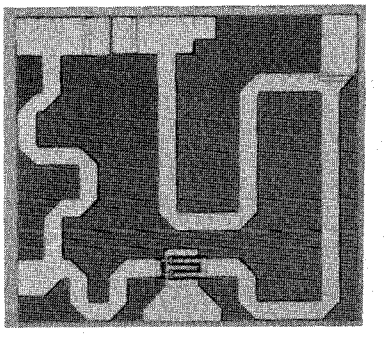

Fig. 4 One-stage amplifier chip photograph

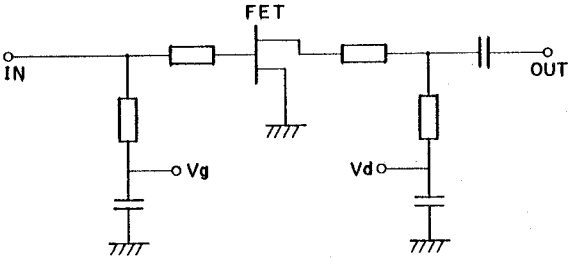

Fig. 5 One-stage amplifier equivalent circuit

There are two different versions of the two-stage amplifier. One is constructed through cascaded connection between two identical one-stage amplifiers, as shown in Fig. 6. Therefore, the chip is double sized at 2 mm x 0.9 mm. In this version, the impedance locus from first to second stage FET passes through a 50Ω point. This route is obviously roundabout. Therefore, chip size reduction can be expected by modifying the interstage matching circuit as the route becomes shortest. In the other version, the modification was carried out by using the CAD program. A chip photograph and its equivalent circuit for the modified version are shown in Fig. 7 and Fig. 8, respectively. As shown, the chip size is reduced to 1.5 mm x 0.9 mm, although matching element sensitivity becomes somewhat higher. Gate bias voltage for the second stage FET is supplied through a resister. The resistance was chosen larger than 5KΩ to prevent causing dissipation loss.

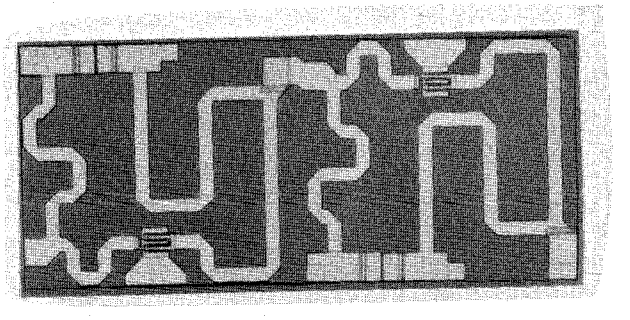

Fig. 6 Cascaded version two-stage amplifier chip photograph

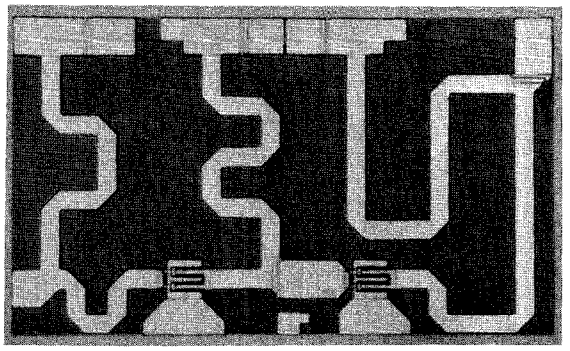

Fig. 7 Modified version two-stage amplifier chip photograph

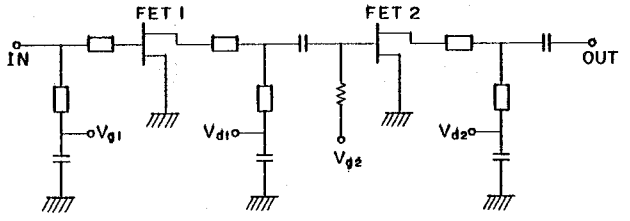

Fig. 8 Modified version two-stage amplifier equivalent circuit

FABRICATION PROCESS

Fig. 9 shows a cross-section view for various circuit elements together with their equivalent circuit. A Cr-doped semi-insulating HB-grown GaAs wafer is selectively implanted with $^{30}Si^{+}$ to form FET active layers. Resistive layers are formed at the same time. Implanting conditions for realizing V_T = -1.7 V are 70 keV energy and 3.2 x 10^{12} cm^{-2} dose. The wafer is then annealed with 0.2 um thick CVD-SiO_2 cap at 800 ° C for 20 minutes in a H_2 ambient. Al, which is used as FET gates and capacitor lower electrodes, is evaporated to 0.4 um thickness and etched to form the gates. Ohmic electrodes for the FETs and the resistors are then formed by lifting-off a AuGe-Ni film and alloying at 400 ° C.

In GaAs IC fabrication, the gate forming process is usually most difficult. In this process, however, it is very simple because the gates and the ohmic electrodes are self-aligned, as previously mentioned. The Al is again etched to form the capacitor lower electrodes. SiO_2 for FET passivation and capacitor dielectric material is chemically-vapor-deposited to 0.2 um thickness and etched to form contact vias. Ti for electro-plating feeder is evaporated onto the whole wafer. Microstrip lines and capacitor upper electrodes are then formed by Ti-Pt-Au lifting-off and thickened to 2.5 um by selective Au plating. Topside processing is completed by etching off the feed metal Ti. The wafer is thinned and the rear is metallized by AuGe · Ni-Au evaporation. Amplifier chips can be obtained by scribing the wafer.

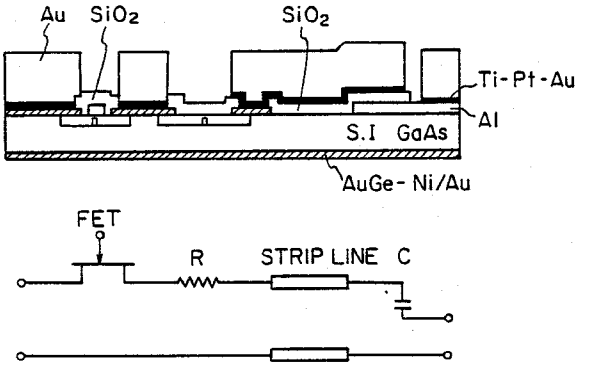

Fig. 9 Circuit elements cross-section view and equivalent circuit

MICROWAVE PERFORMANCE

Amplifier chips were chosen for microwave evaluation on the basis of visual inspection and DC testing. The selected chips were mounted on Au plated copper carriers using AuSn solder. The carriers were then mounted on test fixtures and tested in a 50Ω system. Needless to say, no external bias tee is necessary, because bias circuits are included on the chips.

Fig. 10 shows gain and noise figure characteristics for the one-stage amplifier. In the 11.7 to 12.7 GHz band, which is the desired frequency band, the amplifier provides less than 2.5dB noise figure with more than 9.5dB associated gain. The maximum gain and the minimum noise figure in the band are 12dB and 2.2dB, respectively. Bias conditions are 2.5 V drain voltage and 10mA drain current. Although the gain can be increased by increasing the drain voltage, as well as the drain current, when this increase is made the noise figure is degraded. The noise figure was measured by using a mixer at 70 MHz IF frequency. Input and output VSWRs are less than 3 and less than 2.5 in the desired frequency band, respectively.

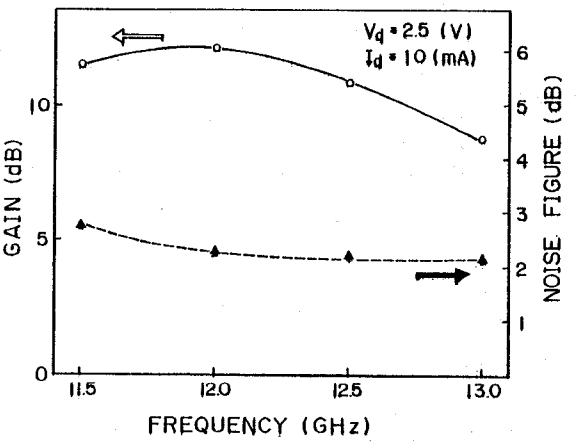

Fig. 10 One-stage amplifier gain and noise figure characteristics

Gain and noise figure characteristics for the cascaded version two-stage amplifier are shown in Fig. 11. More than 20dB gain with 24dB maximum and less than 3dB noise figure with 2.6dB minimum are obtained in the desired band. Input VSWR is less than 4 and output VSWR is less than 2.5. These characteristics mostly agree with prediction values from the one-stage amplifier, because this version is constructed simply by the cascaded connection. For two-stage amplifiers, drain current for the second stage FET is set at 15mA.

Fig. 12 shows gain and noise figure characteristics for the modified version two-stage amplifier. In the desired frequency band, the amplifier has a less than 2.8dB noise figure with more than 16dB associated gain. Although the gain is degraded, compared with the cascaded version, the noise figure is improved. Input and output impedances for this amplifier are shown in Fig. 13. In the figure, reference planes are chosen at scribed edges of the amplifier chip. Less than 2.5 input VSWR and less than 2 output VSWR are obtained in the 11.7 to 12.7 GHz band. These performances are well within the acceptable range for DBS receivers.

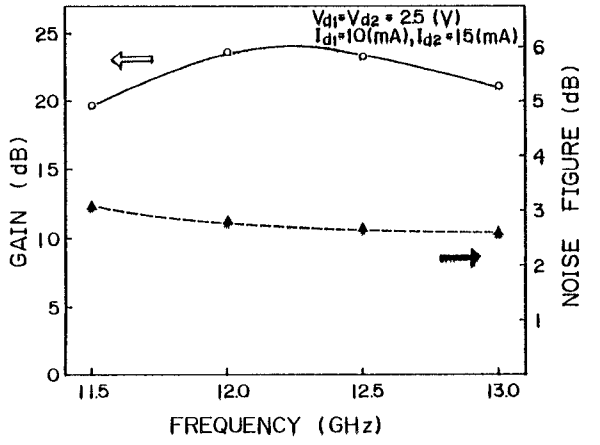

Fig. 11 Cascaded version two-stage amplifier gain and noise figure characteristics

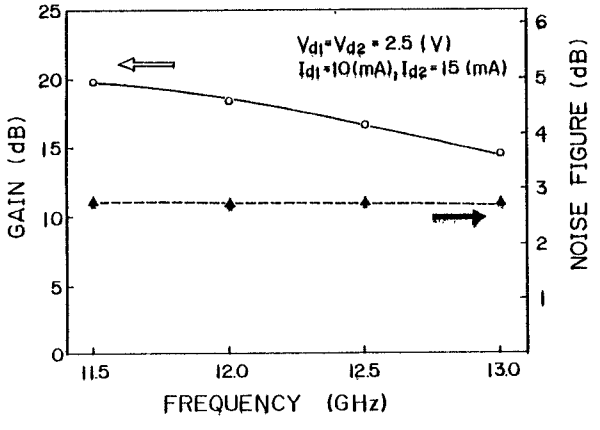

Fig. 12 Modified version two-stage amplifier gain and noise figure characteristics

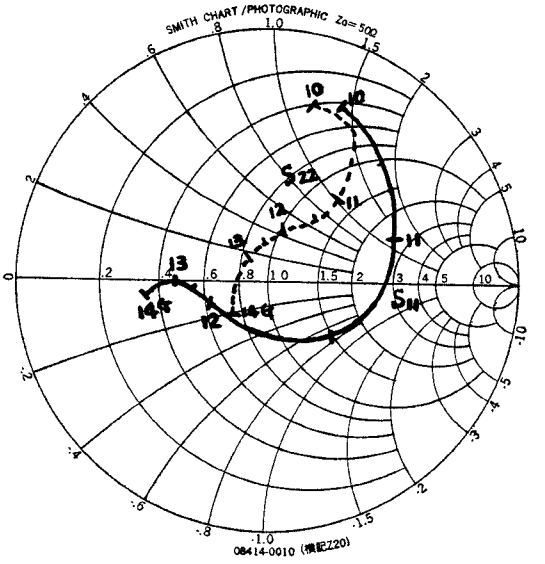

Fig. 13 Modified version two-stage amplifier input and output impedances

CONCLUSION

The design considerations, fabrication process and performances for newly developed one- and two-stage 12GHz-band low-noise GaAs monolithic amplifiers for use in DBS receivers have been described. By introducing the CSE FET, both low noise figure and improved reproducibility can be achieved. Chip size reduction is also accomplished by employing the compact matching circuits. The measured microwave performances are well within the acceptable range for DBS receivers. Although the investigation on yield is not sufficient, it is believed that this approach has a potential to obtain a good result. This work has made a cost-effective one-chip frontend for DBS systems more realistic.

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REFERENCES

(1) K. Kermarrec, P. Harrop, C. Tsironis and J. Faguat, "Monolithic Circuits for 12GHz Direct Broadcasting Satellite Reception", Microwave and Millimeter-Wave Monolithic Circuits Symp. Digest of Papers, pp. 5-10, June 1982.

(2) L.C. Liu, D.W. Maki, M.Feng and M. Siracusa, "Single and Dual Stage Monolithic Low Noise Amplifiers", GaAs IC Symp. Technical Digest, pp. 94-97, Nov. 1982.

(3) T. Furutsuka, T. Tsuji, F. Katano, A. Higashisaka and K. Kurumada, "Ion-Implanted E/D Type GaAs IC Technology", Electron. Letts. vol. 17, No. 25/26, pp. 944-945, Dec. 1981.
(4) K. Honjo, T. Sugiura, T. Tsuji and T. Ozawa, "Low-Noise Low-Power-Dissipation GaAs Monolithic Broadband Amplifiers", GaAs IC Symp. Technical Digest, pp. 87-90, Nov. 1982.
(5) K. Ohata, H. Itoh, F. Hasegawa and Y. Fujiki, "Super Low-Noise GaAs MESFET's with a Deep-Recess Structure", IEEE Trans. on Electron Devices, vol. ED-27, No. 6, pp. 1029-1034, June 1980.